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Zilka-Kotab, PC
P.O. BOX 721120
SAN JOSE, CA 95172-1120

EXAMINER
AMIN, JWALANT B

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/006,551	DONHAM ET AL.
	Examiner	**Art Unit**	
	Jwalant Amin	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>20 June 2007</u>.

2a)☒ This action is **FINAL.**   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-30</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-30</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments filed 6/20/07 have been fully considered but they are not

persuasive.

2.   Regarding claims 1-12, 18-21, 24-29 and 30, the applicant argues that Rivard

does not recognize "to accommodate the programmability of recent texture and shader

modules without being inhibited by the size of associated programs" (see page 5 first

paragraph of applicant's remarks).

3.   In response to applicant's argument that the references fail to show certain

features of applicant's invention, it is noted that the features upon which applicant relies

(i.e., to accommodate the programmability of recent texture and shader modules without

being inhibited by the size of associated programs) are not recited in the rejected

claim(s). Although the claims are interpreted in light of the specification, limitations from

the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26

USPQ2d 1057 (Fed. Cir. 1993).

4.   Regarding claims 1-12, 18-21, 24-29 and 30, the applicant repetitiously argue

that Rivard fails to teach "sending an instruction to memory utilizing a texture module in

a graphics pipeline" (see pg. 7 paragraph two of applicant's remarks).

5.   However, the examiner interprets that Rivard (Fig. 6, Fig. 10, col. 4 lines 46-57,

col. 6 lines 45-67, col. 7 lines 1-10) teaches sending an instruction request to video

memory, where a texture module in a graphics pipeline sends the instruction request to

the video memory (a texture mapping stage sends information to texel cache system;

the texture mapping stage and the texel cache system together are considered as texture module, so the information is passed between the components of the texture module; texel cache system comprising the memory request generator, pipeline latency elements, and cache data store and memory data resolver forwards the memory requests/read requests to DRAM for information retrieval. the examiner interprets that Rivard discloses sending an instruction request to video memory by generating memory request for all misses, and forwards the requests to DRAM for information retrieval (Fig. 6, Fig. 10, col. 4 lines 46-57, col. 6 lines 45-67, col. 7 lines 1-10). It is interpreted that an instruction request could be considered as merely a request because it is basically a request that requires DRAM to perform necessary operation. The examiner also interprets that instructions stored in DRAM that are requested are basically stored as data. It is further interpreted that memory requests/read requests act as an instruction to DRAM based on which DRAM performs a particular function. Memory requests/read requests for all misses that are forwarded to DRAM are instruction requests based on which DRAM sends back information; the examiner relies on the definition of instruction provided by dictionary.com, which defines instructions as a command given to a computer to carry out a particular operation and can contain data to be used in the operation; here DRAM sends memory data based on the memory requests/read requests from the texture module.

6.   Regarding claims 1-12, 18-21, 24-29 and 30, the applicant repetitiously argue that Rivard fails to teach "receiving instructions from the video memory in response to

the instruction request utilizing the texture module in the graphics pipeline" (see pg. 11

paragraph two of applicant's remarks).

7.   In response to applicant's arguments against the references individually, one

cannot show nonobviousness by attacking references individually where the rejections

are based on combinations of references. See In re Keller, 642 F.2d 413, 208

USPQ 871 (CCPA 1981); In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir.

1986).

In this case, the examiner interprets that Rivard (Fig. 6, Fig. 10, col. 4 lines 46-

57, col. 6 lines 45-67, col. 7 lines 1-10) teaches sending an instruction request to video

memory, where a texture module in a graphics pipeline sends the instruction request to

the video memory (a texture mapping stage sends information to texel cache system;

the texture mapping stage and the texel cache system together are considered as

texture module, so the information is passed between the components of the texture

module; texel cache system comprising the memory request generator, pipeline latency

elements, and cache data store and memory data resolver forwards the memory

requests/read requests to DRAM for information retrieval. the examiner interprets that

Rivard discloses sending an instruction request to video memory by generating memory

request for all misses, and forwards the requests to DRAM for information retrieval (Fig.

6, Fig. 10, col. 4 lines 46-57, col. 6 lines 45-67, col. 7 lines 1-10). It is interpreted that an

instruction request could be considered as merely a request because it is basically a

request that requires DRAM to perform necessary operation. The examiner also

interprets that instructions stored in DRAM that are requested are basically stored as

data. It is further interpreted that memory requests/read requests act as an instruction to

DRAM based on which DRAM performs a particular function. Memory requests/read

requests for all misses that are forwarded to DRAM are instruction requests based on

which DRAM sends back information; the examiner relies on the definition of instruction

provided by dictionary.com, which defines instructions as a command given to a

computer to carry out a particular operation and can contain data to be used in the

operation; here DRAM sends memory data based on the memory requests/read

requests from the texture module.

Rivard further teaches receiving instructions from the video memory in response

to the instruction request utilizing the texture module in the graphics pipeline (it is

interpreted that instructions stored in DRAM that are requested are basically stored as

data, and Rivard teaches to send back data in some form in response to the memory

request generated as a result of a miss; DRAM returns memory data to cache data

store and memory data resolver component of texel cache system, which further sends

this information to the texture mapping stage; the texture mapping stage and the texel

cache system together are considered as texture module, so the information/memory

data is passed between the components of the texture module).

Although Rivard discloses the limitations as stated above, Rivard does not

explicitly teach to combine texture mapping stage and texel cache system to form a

texture module. However, it would have been obvious to one of ordinary skill in art at

the time of present invention to combine texture mapping stage and texel cache system

of Rivard to work together as a texture module. The unity of diversity of parts would

depend more upon the choice of the manufacturer, and the convenience and availability

of the machines and tools necessary to construct the texture module, than on any

inventive concept. One of ordinary skill in art, furthermore, would have expected

applicant's invention to perform equally well with Rivard's reference that teaches to

send and receive information/instruction from the texture mapping stage and texel

cache system to the DRAM because using this components together will also result in

sending and receiving instructions to and from DRAM. Therefore, it would have been

obvious to one of ordinary skill in art at the time of present invention to modify Rivard to

obtain the invention as specified in the claim.

The examiner further interprets that Rivard also teaches the arrival of memory

data and associated instructions at the cache data store and memory data resolver

component of the text cache system is coordinated by pipeline latency elements (col. 7

lines 4-7; memory data has associated instructions; however, Rivard does not explicitly

state that the data and it's associated instructions are returned by DRAM, though the

data has it's associated instructions). Therefore, the examiner brings in the Wang

reference that suggests a graphics subunit (texture module) in a graphics hardware

system that supplies data and control signals to local frame buffer memory for executing

a series of display instructions (Fig. 1, col. 5 lines 38-67; the computer memory includes

the local frame buffer memory, which corresponds to the DRAM; based on the control

signals send by the graphics hardware system, the frame buffer returns the polygon

display instructions that includes the texture data, so that the graphics subunit executes

the display instructions using this data). Therefore, it would have been obvious to one of

ordinary skill in art at the time of present invention to have the memory return

instructions as taught by Wang to the texture module of Rivard because these

instructions are needed to render the graphics primitives to be displayed on the display

device (col. 5 lines 43-45 and lines 63-67).

8.   Regarding claims 1-12, 18-21, 24-29 and 30, the applicant argues that it would

not have been obvious to "combine texture mapping stage and texel cache system"

(see pg. 12 last line and pg. 13 first line of applicant's remarks).

9.   However, the examiner interprets that although Rivard does not explicitly teach to

combine texture mapping stage and texel cache system to form a texture module, it

would have been obvious to one of ordinary skill in art at the time of present invention to

combine texture mapping stage and texel cache system of Rivard to work together as a

texture module. The unity of diversity of parts would depend more upon the choice of

the manufacturer, and the convenience and availability of the machines and tools

necessary to construct the texture module, than on any inventive concept. One of

ordinary skill in art, furthermore, would have expected applicant's invention to perform

equally well with Rivard's reference that teaches to send and receive

information/instruction from the texture mapping stage and texel cache system to the

DRAM because using this components together will also result in sending and receiving

instructions to and from DRAM. Therefore, it would have been obvious to one of

ordinary skill in art at the time of present invention to modify Rivard to obtain the

invention as specified in the claim. See *In re Lockhart, 90 USPQ (CCPA 1951).*

10.   Regarding claims 1-12, 18-21, 24-28 and 30, the applicant argues that Wang

does not disclose "receiving instructions ... utilizing the texture module in the graphics

pipeline" (see pg. 13 last two lines of applicant's remarks),

11.   However, the examiner interprets that Rivard teaches to send a request to DRAM

via a texture module, and based on this request, DRAM sends back data and it's

associated information to the texture module (see the arguments above for details).

Nonetheless, Rivard does not explicitly state that the data and it's associated

instructions are returned by DRAM, though the data has it's associated instructions.

Therefore, the examiner brings in the Wang reference that suggests a graphics subunit

(texture module) in a graphics hardware system that supplies data and control signals to

local frame buffer memory for executing a series of display instructions (Fig. 1, col. 5

lines 38-67; the computer memory includes the local frame buffer memory, which

corresponds to the DRAM; based on the control signals send by the graphics hardware

system, the display list stored in the frame buffer returns the polygon display

instructions that includes the texture data, so that the graphics subunit executes the

display instructions using this data). Therefore, it would have been obvious to one of

ordinary skill in art at the time of present invention to have the memory return

instructions as taught by Wang to the texture module of Rivard because these

instructions are needed to render the graphics primitives to be displayed on the display

device (col. 5 lines 43-45 and lines 63-67).

12.   Regarding claim 28, the applicant argues that Rivard fails to meet applicant's

claimed "receiving additional instructions utilizing the texture module" (see pg. 17 first

paragraph of applicant's remarks).

13.   In response to applicant's arguments against the references individually, one

cannot show nonobviousness by attacking references individually where the rejections

are based on combinations of references. See In re Keller, 642 F.2d 413, 208

USPQ 871 (CCPA 1981); In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir.

1986).

In this case, the examiner interprets that Rivard teaches a texture mapping stage

as shown in Fig. 6 receiving data (instructions) from the rasterizer module of the

pipeline and then receiving data (data and it's associated instructions) from the DRAM.

The instructions received from the rasterizer module are considered to be the first

instructions, and thus the instructions received from the DRAM via the texel cache

system are considered to be the additional instructions.

Since Rivard does not explicitly state that the data and it's associated instructions

are returned by DRAM, though the data has it's associated instructions, the examiner

relies on the Wang reference that suggests a graphics subunit (texture module) in a

graphics hardware system that supplies data and control signals to local frame buffer

memory for executing a series of display instructions (Fig. 1, col. 5 lines 38-67; the

computer memory includes the local frame buffer memory, which corresponds to the

DRAM; based on the control signals send by the graphics hardware system, the display

list stored in the frame buffer returns the polygon display instructions that includes the

texture data, so that the graphics subunit executes the display instructions using this data). Therefore, it would have been obvious to one of ordinary skill in art at the time of present invention to have the memory return instructions as taught by Wang to the texture module of Rivard because these instructions are needed to render the graphics primitives to be displayed on the display device (col. 5 lines 43-45 and lines 63-67).

14.   Regarding claim 29, the applicant argues that Rivard fails to meet applicant's claimed "sending an instruction request utilizing a texture module coupled to the shader module" (see pg. 18 lines 3-5 of applicant's remarks). The applicant further argues that AAPA does not teach "sending an instruction request to video memory, where a texture module coupled to the shader module sends the instruction request to the video memory" (see pg. 18 first paragraph of applicant's remarks).

15.   In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In this case, the examiner interprets that Rivard, in view of Wang teaches to send an instruction request to memory utilizing a texture module (see refer to the arguments above for details).

Although the combination of Rivard and Wang teach a method and system for retrieving instructions from memory utilizing a texture module in a graphics pipeline, they do not explicitly teach controlling the texture module utilizing a shader module

coupled thereto. However, AAPA teaches controlling the texture module utilizing a

shader module coupled thereto (Fig.3; shader module is also coupled to the rasterizer

module). Therefore, it would have been obvious to a person of ordinary skill in the art at

the time of the invention to incorporate the shading module of AAPA into the texture

module of Rivard and Wang because combination of shading module and texture

module would enable a shading function to the graphic pipeline.

16.   Regarding claim 18, the applicant argues that Wang does not teach "a complete

instruction set is received in response to the instruction request where the instructions

are received from the video memory" (see pg. 22 first paragraph of applicant's remarks).

17.   Regarding claim 18, Rivard does not explicitly teach a complete instruction set is

received in response to the instruction request. However, Wang (col. 5 lines 43-67, col.

6 lines 1-47) teaches a graphics subunit (texture module) of a graphics hardware

system executing a series of display instructions (set of instructions) stored in computer

memory (Fig. 1, col. 5 lines 38-67; the computer memory includes the local frame buffer

memory, which corresponds to the DRAM; based on the control signals send by the

graphics hardware system, the display list stored in the frame buffer returns the polygon

display instructions that includes the texture data, so that the graphics subunit executes

the display instructions using this data). The graphics subunit receives display

instructions including texture data based on the supplied data and control signals (the

examiner interprets that the claims do not specify how many instructions are needed to

make a set complete; the examiner interprets that if the required operation can be

performed from just the one received instruction, then it is considered as a complete set

of instruction; the single display instruction received by the graphics from the sub-routine process in response to the control signals correspond to a complete set of instruction; this instruction in the sub-routine is executed by the graphics subunit for rendering the concerned graphics primitive, and therefore it is considered as a complete set of instruction). Therefore, it would have been obvious to one of ordinary skill in art at the time of present invention to have the memory return a complete set of instructions as taught by Wang to the texture module of Rivard because this instruction set is needed to render the concerned graphics primitive (col. 5 lines 43-45 and lines 63-67).

18.   Regarding claim 19, the applicant argues that Wang does not teach "a partial instruction set is received in response to the instruction request where the instructions are received from the video memory" (see pg. 22 first paragraph of applicant's remarks).

19.   Regarding claims 19, Rivard does not explicitly teach a partial instruction set is received in response to the instruction request. However, Wang (col. 5 lines 43-67, col. 6 lines 1-47) teaches a graphics subunit (texture module) of a graphics hardware system executing a series of display instructions (set of instructions) stored in computer memory. The graphics subunit receives display instructions including texture data based on the supplied data and control signals (the examiner interprets that the claims do not specify how many instructions are needed to make a set complete or partial; the examiner interprets that if the required operation can be performed from just the one received instruction, then it is considered as a complete set of instruction; however, the rendering process might need other instructions for rendering other primitives, and in this case, the single received instruction is considered as a partial set of instruction; the

single display instruction received by the graphics from the sub-routine process in

response to the control signals correspond to a partial set of instruction; this instruction

in the sub-routine is executed by the graphics subunit for rendering the concerned

graphics primitive, but other instructions are needed for rendering other primitives, and

therefore overall this single instruction is considered as a partial set of instruction).

Therefore, it would have been obvious to one of ordinary skill in art at the time of

present invention to have the memory return instructions as taught by Wang to the

texture module of Rivard because these instructions are needed to render the graphics

primitives to be displayed on the display device (col. 5 lines 43-45 and lines 63-67).

Claim Rejections - 35 USC § 103

20.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

21.   Claims 1-12, 18-21, 24-28 and 30 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Rivard (US 5,987,567), and in view of Wang (5,831,640).

22.   Regarding claims 1, 21, 24-27 and 30, Rivard (Fig. 6, Fig. 10, col. 4 lines 46-57,

col. 6 lines 45-67, col. 7 lines 1-10) teaches a method for execution with a system

including a tangible computer readable medium, the method for retrieving instructions

from video memory (DRAM 655) utilizing a texture module (texture mapping stage 645

and texel cache system 650 combined together corresponds to texture module) in a

graphics pipeline (graphics pipeline 640), comprising

sending an instruction request to video memory, where a texture module in a

graphics pipeline sends the instruction request to the video memory (a texture mapping

stage sends information to texel cache system; the texture mapping stage and the texel

cache system together are considered as texture module, so the information is passed

between the components of the texture module; texel cache system comprising the

memory request generator, pipeline latency elements, and cache data store and

memory data resolver forwards the memory requests/read requests to DRAM for

information retrieval (the examiner interprets that memory requests/read requests for all

misses that are forwarded to DRAM are instruction requests based on which DRAM

sends back information; the examiner relies on the definition of instruction provided by

dictionary.com, which defines instructions as a command given to a computer to carry

out a particular operation and can contain data to be used in the operation; here DRAM

sends memory data based on the memory requests/read requests from the texture

module. Memory requests/read requests act as an instruction to DRAM, which performs

a particular function based on the request); and

receiving instructions from the video memory in response to the instruction

request utilizing the texture module in the graphics pipeline (DRAM returns memory

data to cache data store and memory data resolver component of texel cache system,

which further sends this information to the texture mapping stage; the texture mapping

stage and the texel cache system together are considered as texture module, so the information/memory data is passed between the components of the texture module).

Although Rivard discloses the limitations as stated above, Rivard does not explicitly teach to combine texture mapping stage and texel cache system to form a texture module. However, it would have been obvious to one of ordinary skill in art at the time of present invention to combine texture mapping stage and texel cache system of Rivard to work together as a texture module. The unity of diversity of parts would depend more upon the choice of the manufacturer, and the convenience and availability of the machines and tools necessary to construct the texture module, than on any inventive concept. One of ordinary skill in art, furthermore, would have expected applicant's invention to perform equally well with Rivard's reference that teaches to send and receive information/instruction from the texture mapping stage and texel cache system to the DRAM because using this components together will also result in sending and receiving instructions to and from DRAM. Therefore, it would have been obvious to one of ordinary skill in art at the time of present invention to modify Rivard to obtain the invention as specified in the claim.

Rivard also teaches the arrival of memory data and associated instructions at the cache data store and memory data resolver component of the text cache system is coordinated by pipeline latency elements (col. 7 lines 4-7; memory data has associated instructions). Although Rivard discloses the limitations as stated above, Rivard does not explicitly teach that the memory returns instructions along with data, in response to instruction request from the texture module. However, Wang teaches a graphics subunit

(texture module) in a graphics hardware system that supplies data and control signals to local frame buffer memory for executing a series of display instructions (Fig. 1, col. 5 lines 38-67; the computer memory includes the local frame buffer memory, which corresponds to the DRAM; based on the control signals send by the graphics hardware system, the frame buffer returns the polygon display instructions that includes the texture data, so that the graphics subunit executes the display instructions using this data). Therefore, it would have been obvious to one of ordinary skill in art at the time of present invention to have the memory return instructions as taught by Wang to the texture module of Rivard because these instructions are needed to render the graphics primitives to be displayed on the display device (col. 5 lines 43-45 and lines 63-67).

23.   Regarding claim 2, Rivard teaches a method and system for retrieving instructions from memory utilizing a texture module in a graphics pipeline, comprising sending a texture request (texture lookup requests) to memory utilizing the texture module in the graphics pipeline (Fig. 6, col. 6 lines 50-60).

24.   Regarding claim 3, Rivard teaches receiving texture information (memory data) from the memory in response to the texture request utilizing the texture module in the graphics pipeline (Fig. 6, col. 6 lines 50-56).

25.   Regarding claim 4, Rivard teaches the video memory includes a frame buffer (col. 3 lines 5-10).

26.   Regarding claim 5, Rivard teaches the memory includes direct random access memory (DRAM) (col.4 lines 32-35 and lines 45-55).

27.   Regarding claim 6, Rivard teaches the instructions are adapted for controlling a

texture environment module (pipeline latency elements) coupled to the texture module

(Fig.6, Fig.10).

28.   Regarding claim 7, Rivard teaches the instructions control the manner in which

the texture environment module processes the texture information (col.7 lines 3-7).

29.   Regarding claim 8, Rivard teaches receiving initial instructions from a rasterizer

module (graphic accelerator having graphic pipeline stage shows that the texture

module receives data/instructions from the upper modules of the pipeline) coupled to

the texture module (Fig.6).

30.   Regarding claim 9, Rivard teaches the initial instructions control at least the

sending of the instruction request by the texture module (Fig. 6; graphic accelerator

having graphic pipeline stage shows that the texture module receives data/instructions

from the upper modules of the pipeline; thus based on these instructions, the texture

module sends the instruction request to the DRAM).

31.   Regarding claim 10, Rivard teaches temporarily storing the instructions and the

texture information in cache (cache data store and memory data resolver) (Fig. 6, Fig.

10).

32.   Regarding claim 11, Rivard teaches the cache is resident on the texture module

(Fig.6, Fig.10).

33.   Regarding claim 12, Rivard teaches that each piece of texture information and

each of the instructions are of a similar size in the memory (col. 6 lines 50-67 and col. 7

lines 1-15; texture mapping stage includes the ALU which reformats data including resizing of texel data types for uniformity).

34. Regarding claim 18, although Rivard teaches the above-discussed limitations, Rivard does not explicitly teach a complete instruction set is received in response to the instruction request. However, Wang (col. 5 lines 43-67, col. 6 lines 1-47) teaches a graphics subunit (texture module) of a graphics hardware system executing a series of display instructions (set of instructions) stored in computer memory. The graphics subunit receives display instructions including texture data based on the supplied data and control signals (the single display instruction received by the graphics from the sub-routine process in response to the control signals correspond to a complete set of instruction; this instruction in the sub-routine is executed by the graphics subunit for rendering the concerned graphics primitive, and therefore it is considered as a complete set of instruction). Therefore, it would have been obvious to one of ordinary skill in art at the time of present invention to have the memory return a complete set of instructions as taught by Wang to the texture module of Rivard because this instruction set is needed to render the concerned graphics primitive (col. 5 lines 43-45 and lines 63-67).

35. Regarding claims 19, although Rivard teaches the above-discussed limitations, Rivard does not explicitly teach a partial instruction set is received in response to the instruction request. However, Wang (col. 5 lines 43-67, col. 6 lines 1-47) teaches a graphics subunit (texture module) of a graphics hardware system executing a series of display instructions (set of instructions) stored in computer memory. The graphics subunit receives display instructions including texture data based on the supplied data

and control signals (the single display instruction received by the graphics from the sub-routine process in response to the control signals correspond to a partial set of instruction; this instruction in the sub-routine is executed by the graphics subunit for rendering the concerned graphics primitive, but other instructions are needed for rendering other primitives, and therefore overall this single instruction is considered as a partial set of instruction). Therefore, it would have been obvious to one of ordinary skill in art at the time of present invention to have the memory return instructions as taught by Wang to the texture module of Rivard because these instructions are needed to render the graphics primitives to be displayed on the display device (col. 5 lines 43-45 and lines 63-67).

36.   Regarding claim 20, the statements presented above, with respect to claims 1 and 19, are incorporated herein.

37.   Regarding claim 28, Rivard teaches a texture mapping stage as shown in Fig. 6 receiving data (instructions) from the rasterizer module of the pipeline and then receiving data (instructions) from the DRAM. Thus the instructions received from the DRAM via the texel cache system are considered to be the additional instructions. Please refer to the rejection of claims 1, 2, 3, 8 and 10 for further details regarding the rejection of other limitations.

38.   Claims 13-17, 22, 23, 29, are rejected under 35 U. S.C. 103(a) as being unpatentable over Rivard and Wang, and further in view of Applicant Admitted Prior Art (AAPA).

39.   Regarding claim 13, although the combination of Rivard and Wang teach a

method and system for retrieving instructions from memory utilizing a texture module in

a graphics pipeline, they do not explicitly teach controlling the texture module utilizing a

shader module coupled thereto. However, AAPA teaches controlling the texture module

utilizing a shader module coupled thereto (Fig.3; shader module is also coupled to the

rasterizer module). Therefore, it would have been obvious to a person of ordinary skill in

the art at the time of the invention to incorporate the shading module of AAPA into the

texture module of Rivard and Wang because combination of shading module and

texture module would enable a shading function to the graphic pipeline.

40.   Regarding claim 14, although the combination of Rivard and Wang teach a

method and system for retrieving instructions from memory utilizing a texture module in

a graphics pipeline, they do not explicitly teach the shader module controls the sending

of instruction request and texture request by the texture module. However, AAPA

teaches this limitation (Fig. 3 page 5 lines 24-31).

41.   Regarding claim 15, although the combination of Rivard and Wang teach a

method and system for retrieving instructions from memory utilizing a texture module in

a graphics pipeline, they do not explicitly teach the shader module processes a plurality

of pixels with the texture information based on the instructions. However, AAPA teaches

this limitation (Fig. 3).

42.   Regarding claim 16, although the combination of Rivard and Wang teach a

method and system for retrieving instructions from memory utilizing a texture module in

a graphics pipeline, they do not explicitly teach the shader module is capable of reusing

the texture information in order to request further texture information from the video

memory (control the looping of texture process). However, AAPA teaches this limitation

(Fig. 3 page 4 lines 24-31).

43.   Regarding claim 17, although the combination of Rivard and Wang teach a

method and system for retrieving instructions from memory utilizing a texture module in

a graphics pipeline, they do not explicitly teach ceasing the processing upon the receipt

of terminate instruction (require significant amount of time to push down the pipeline).

However, AAPA teaches this limitation (Fig. 3 page 5 lines 7-15).

44.   Regarding claims 22, 23, although the combination of Rivard and Wang teach a

method and system for retrieving instructions from memory utilizing a texture module in

a graphics pipeline, they do not explicitly teach the texture module is adapted for

operating in a plurality of different modes. However, AAPA teach texture module is

adapted for operating in a plurality of different modes. See page 3 lines 20-25. It would

have been obvious to a person of ordinary skill in the art at the time of the invention to

incorporate texture module of Rivard into the texture module of AAPA because a

combination of texture module operating in plurality of difference modes and the texture

module of Rivard would provide components of the texture module processing the

texels in various ways such as an address calculation module allow various

dimensionality textures.

45.   Regarding claim 29, the statements presented above, with respect to claims 1, 2,

3, 8, 10, 13, 14, 15, 17 and 28 are included herein.

Conclusion

46.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

- Lindholm et al. (US 6,975,321 B1)

Bunnell (7,038,678 B2)

47.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

48.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Jwalant Amin whose telephone number is 571-272-

2455. The examiner can normally be reached on 9:30 a.m. - 6:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Mark Zimmerman can be reached on 571-272-7653. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

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system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

*** J.A. 9|15|07

MARK ZIMMERMAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600